ADS62PXX EVM

User's Guide

Literature Number: SLAU237
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ADS62PXX EVM

1 Overview

This user's guide gives a general overview of the evaluation module (EVM) and provides a general description of the features and functions to be considered while using this module. This manual is applicable to the ADS62P42/43/44/45, ADS62P22/23/24/25 and ADS62P15/C15 analog to digital converters (ADC), which will be collectively referred to as ADS62PXX. This document should be used in combination with respective ADC data sheet.

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1.1 ADS62PXX EVM Quick-Start Procedure

Using the quick-start procedure, many users can begin evaluating the ADC in a short time. The quick-start uses the default conditions on the EVM as shipped from the factory. If users modify the default jumper settings, this procedure does not apply.

1. The EVM contains a linear power supply solution to provide the necessary voltage rails to the ADC and associated circuits. Simply connect +5 V to P5 and GND to P4. Short P4 and P2 together.
2. Connector J4 (SMA) is connected to the path of the ADC clock input. It is used to connect the ADC clock input with off-board clock source. A low phase-noise sine-wave clock source is recommended for default EVM setting.
3. Connectors J6 (SMA) and J3 (SMA) are used to connect ADC channel A and channel B, respectively with an off-board analog continuous-wave (CW) signal source.
4. Connect the TSW1200 or suitable logic analyzer to J8 to capture the resulting digital data (DDR LVDS format).

2 Circuit Description

2.1 Schematic Diagram

The schematic diagram for the EVM is in Section 6.3.

2.2 ADC Circuit Function

The following sections describe the function of individual circuits. See the relevant data sheet for device operating characteristics.

2.2.1 ADC Operational Mode

By default, the ADC is configured to operate in parallel-mode operation, since jumper (JP11) asserts a 3.3-V state to the ADC reset pin. Consequently, the SW1 reset pushbutton must be pressed only when the device is configured in serial operation mode. Because the ADC is in parallel operation mode, voltages are used to set the ADC configuration modes. Users can use the EVM silkscreen to set the operation modes.

2.2.2 EVM Power Connections

Banana jacks P1 to P6 on the EVM are used to connect the EVM to off-board DC power supplies. Users are given two primary options for connecting the ADC power supplies. By default, the ADC's AVDD and DVDD voltage rails are generated using TI's TPS79633 linear regulators. Their attributes of ultra-low noise and high PSRR make them ideal choices for high speed ADC power supply design. To measure ADC-device current consumption, we've provided a second DC power supply can be directly connected to the ADC. Users can use jumpers JP15 and JP16, detailed in Table 1, to switch between power supply options.

2.2.3 ADC Analog Inputs

By default, the EVM is configured to accept an AC-coupled single-ended input source from SMAs J6 and J3; these correspond to ADC inputs channel A and channel B, respectively. The input path converts the single-ended signal into a differential signal using a 1:1 transformer. The inputs to the ADC must be DC-biased, which is accomplished by using the ADC VCM output.

Using SMA input J3, users can evaluate the ADC using a THS4509 amplifier, which converts a single-ended input into a differential signal while providing 10 dB of signal gain. The output path of the amplifier is AC coupled, and the DC is restored using the ADC VCM output. To use this evaluation path, please follow the steps below.

1. By default, the amplifier path is powered down. To turn on the THS4509, move the jumper found at JP3 to short positions 1-2.
2. Supply 5V DC to VS+ (P5) and connect ground to VS– (P6).
3. For AC-coupled evaluation setups, remove R72. This will force the amplifier common mode to Vss/2.
4. To connect the SMA input J3 to the amplifier inverting input terminal, short positions 2 and 3 on SJP5.
5. To connect the amplifier outputs to the ADC input, short positions 1 and 2 on both SJP1 and SJP2.
6. Components L6, C62, C29, L8, L7, C28, C61, L5 form a bandpass filter with cutoff frequencies of 105 MHz and 185 MHz, respectively. Customers will need to optimize this depending on their usage requirements.

Note that the THS4509 used on this EVM is pinout compatible with the THS4508, THS4511, THS4513, and THS4520. Users can easily interchange the amplifier on this EVM and pick the appropriate amplifier based on common-mode range, power supplies, and frequency of operation. Contact your local Texas Instruments (TI) sales representative for assistance in selection of these amplifiers.

2.2.4 ADC Clock Input

Connect a filtered, low-phase-noise clock input to J4. A 1:1 transformer, T6, converts from a single-ended clock signal to a differential clock signal. Resistor R19 serves as a 50-Ω termination.

2.2.5 ADC Digital Outputs

The DDR LVDS digital output of ADS62PXX EVM is brought to a high-density Samtec connector J8 which can be used for digital capture by a logic analyzer or capture card. Since the ADC also supports a CMOS output, provisions have been made to all for the digital output data to be routed to 40-pin IDC connectors J1 and J2. Connector J1 also supports a third output option, dual-channel multiplexed CMOS output. Users wishing to make use of the CMOS output need to make the modifications listed in the bulleted list. Section 4 details connection options to TI's capture solutions, the TSW1100 and TSW1200.

- Remove resistor packs with the following reference designators: RN7, RN8, RN9, and RN10.
- Install TI's SN74AVC16244 buffer into U12 and U13.

2.2.6 Jumper Selections

The EVM features several different operational modes that can be selectable through jumpers described in Table 1. The EVM also features surface-mount jumpers in cases where either the signal integrity is important or the functions are rarely used. Table 2 summarizes these options.

Table 1. Jumpers

Description	Reference Designator	Default Selection	Optional Selection
THS4509 powerdown selection	JP3	2-3, THS4509 off	THS4509 on
ADS62PXX pin: Control Line 3	JP5	1-2, Logic level low, normal ADC operation	Multiple choices
ADS62PXX pin: Control Line 2	JP6	1-2, Logic level low, normal ADC operation	Multiple choices
ADS62PXX pin: Control Line 1	JP7	1-2, Logic level low, normal ADC operation	Multiple choices
SCLK control, USB or onboard voltage dividers	JP8	1–2, Onboard voltage dividers - use silkscreen for configuration	2–3, USB control
SDATA control, USB or onboard voltage dividers	JP9	1–2, Onboard voltage dividers - use silkscreen for configuration	2–3, USB control
SEN control, USB or onboard voltage dividers	JP10	1–2, Onboard voltage dividers - use silkscreen for configuration	2–3, USB control
ADS62PXX pin: Reset	JP11	1-2, Selects the parallel interface	2-3, selects the SPI interface
SCLK Parallel Mode Control	JP12	Multiple options	Multiple options
SDATA Parallel Mode Control	JP13	Multiple options	Multiple options
SEN Parallel Mode Control	JP14	Multiple options	Multiple options
ADC DVDD power supply selection	JP15	2-3, Uses onboard LDO for ADC DVDD supply	1-2, Selects banana jack P1 for ADC DVDD
ADC AVDD power supply selection	JP16	2-3, Uses onboard LDO for ADC AVDD supply	1-2, Selects banana jack P3 for ADC AVDD

Table 2. Surface-Mount Jumpers

Description	Reference Designator	Default Selection	Optional Selection
Amp output or transformer input	SJP1	2–3, ADC input from SMA input J3	1-2, ADC input from THS4509 positive output
Amp output or transformer input	SJP2	2–3, ADC input from SMA input J9	1-2, ADC input from THS4509 negative output
Amp output or transformer input	SJP3	No connection, open	2–3, THS4509 amplifier positive input
Amp output or transformer input	SJP5	1–2, ADC input from SMA input J3	2–3, THS4509 amplifier negative input

3 TI ADC SPI Control Interface

This section describes the software features accompanying the EVM kit. The TI ADC SPI control software provides full control of the SPI interface, allowing users to write to any of the ADC registers found in the data sheet. For most ADS62PXX performance evaluations, users do not need to use the TI SPI control software to get evaluation results. Users only need to use the ADC SPI control software when the desired feature is inaccessible through the ADC parallel interface mode.

3.1 Installing the ADC SPI Control Software

The ADC SPI control software can be installed on a personal computer by running the setup.exe file located on the CD. This file installs the graphical user interface (GUI) along with the USB drivers needed to communicate to the USB port that resides on the EVM. When prompted, users should allow the Windows® operating system to search for device drivers by checking "Yes, this time only", as seen in Figure 1. It will find the TI ADC SPI interface drivers automatically. After the software is installed, insert the USB cable to the EVM to finnish the installation . The "Found New Hardware" wizard will start, and you must acknowledge that the TI ADC SPI Interface has not passed the Windows® Logo testing as shown in Figure 2. After completion, the TI ADC SPI Interface should show up in the Hardware Device Manager. Figure 3 shows the SPI interface in the Hardware Manager which indicates that it is ready for use.

Note: Before plugging in the USB cable for the first time, install the TI ADC SPI software. The software installs the drivers necessary for USB communication.

Figure 1. Found New Hardware

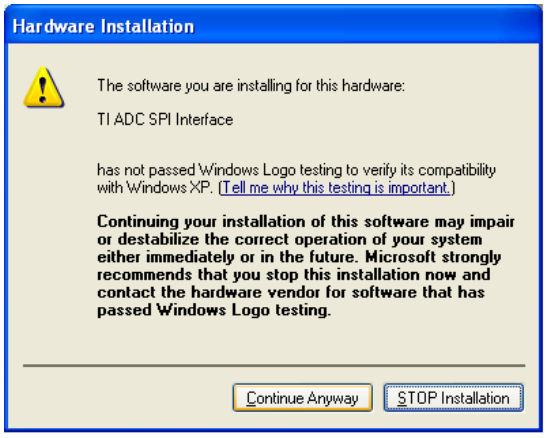

Figure 2. Window Logo Testing

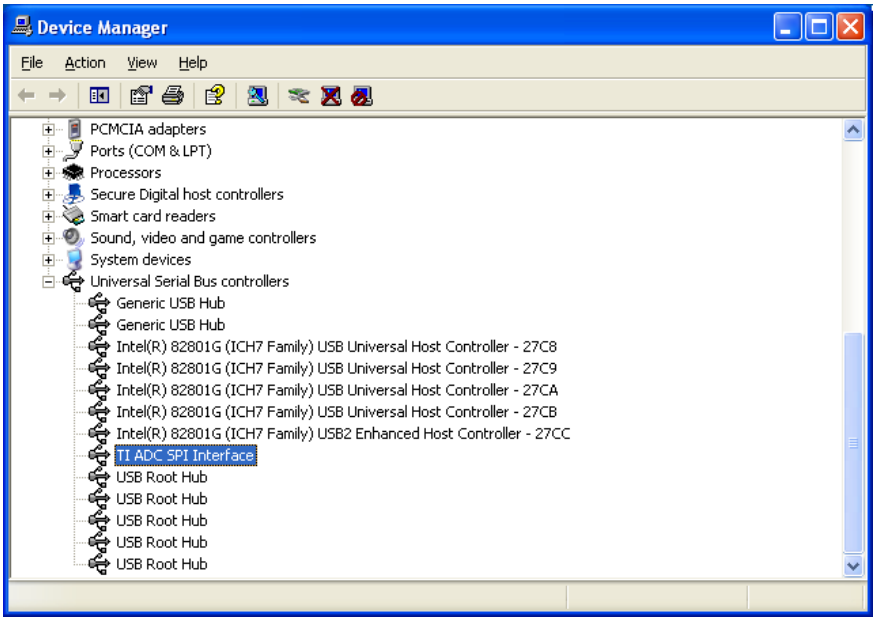

Figure 3. Hardware Device Manager

3.2 Setting Up the EVM for ADC SPI Control

Users who wish to use the ADC SPI interface must supply 5 VDC to P5, which provides power to the USB circuit. By default, the EVM comes with the ADC configured in parallel mode. In order to use the SPI interface to control the ADC modes of operation, users must move several jumpers.

- Move jumper JP11 to short positions 2–3, which places the ADC into serial operation mode.
- Move jumper JP8 to short positions 2–3, which allows the USB circuit to control SCLK.
- Move jumper JP9 to short positions 2–3, which allows the USB circuit to control SDATA.
- Move jumper JP10 to short positions 2–3, which allows the USB circuit to control SEN.

3.3 Using the TI ADC SPI Interface Software

Once the software is installed and the USB cable is connected, three primary modes of operating the software are available: SPI Register Writes, SPI Register Write Using a Script File, and ADS62PXX Frequently Used Registers.

Note: Before beginning and ADC evaluation, users are required to reset the ADC. This can easily be done by pressing the ADS62PXX Reset button found on the ADS62PXX tab. For most ADS62PXX evaluations that make use of the SPI interface, users should also assert the Over-Ride Bit also found on the ADS62PXX tab. This will force the ADC to be configured by the SPI interface only and it will ignore any board-level settings that may have been set. Please consult the datasheet for a full list of available functions in SPI interface mode.

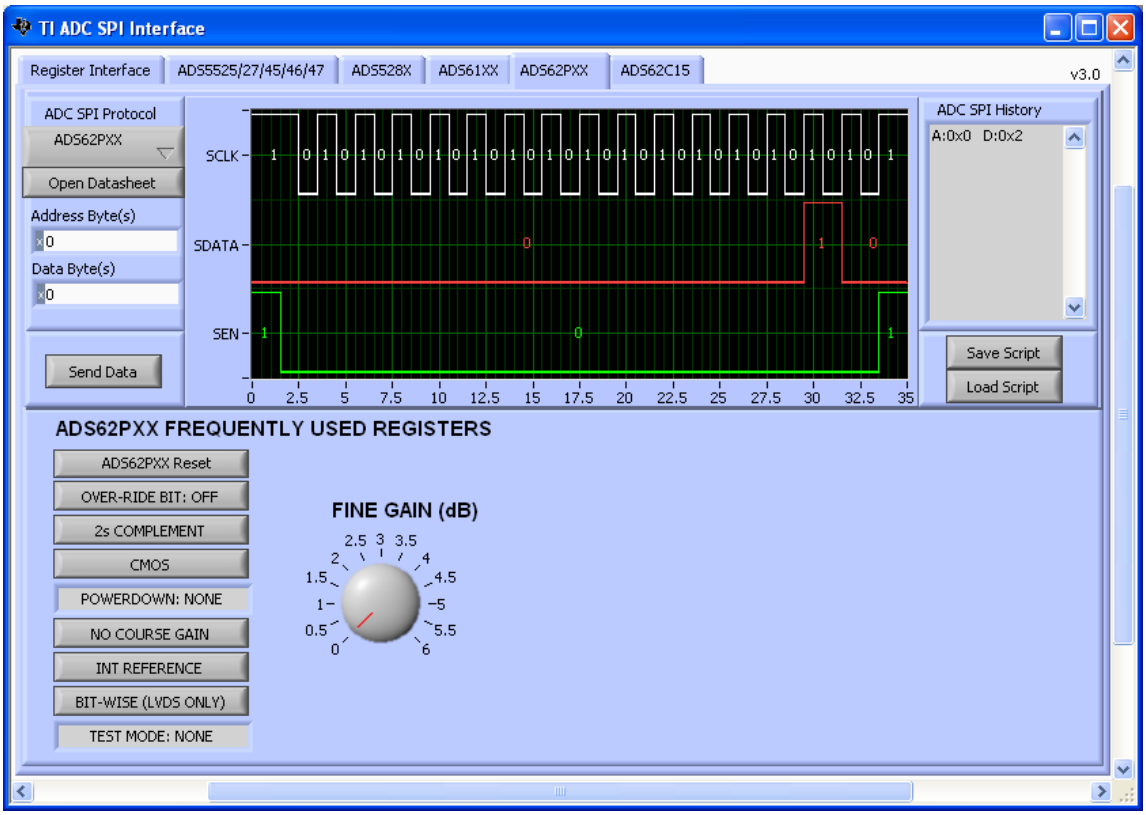

Figure 4. SPI Interface Screen

3.3.1 SPI Register Writes

The most basic mode of operation allows full control of writing to individual register addresses. In the top-left corner of the interface screen (Figure 4), select the ADS62PXX ADC from the ADC SPI Protocol drop-down list. Next, type the Address Bytes(s) in hexadecimal (hex) and Data Byte(s) in hex, which can be found in the device data sheet. When you are ready to send this command to the ADC, either press "Enter" on your keyboard or press the Send Data button. The graph indicator is updated with the patterns sent to the ADC. The default inputs to both the Address Byte(s) and Data Byte(s) fields are hex inputs as designated by the small *x* in the control. Users can change the default input style by clicking on the "x" to binary, decimal, octal, or hex. Multiple register writes can be written simply by changing the contents of the Address Byte(s) and Data Byte(s) field and pressing "Enter" or Send Data again. The ADC SPI History window will keep track of the register writes performed in a session.

3.3.2 SPI Register Write Using a Script File

After the ADC is configured to the desired usage, users can save time in future ADC configurations by saving a script file. By pressing the Save Script button, it dumps ADC SPI History window contents into a text file. Alternatively, users can edit the script file in a text editor. An example script file is located in the \\Install Directory\Script Files\ADS62P45_LVDS_oBinary.txt which configures the ADC for use with the

TSW1200. When ready to write the contents of the script file to the ADC, users can press the Load Script button and they will be prompted for the file location of their script file. The commands are sent to the ADC when the user acknowledges the selection of the file, however the graph indicator does not show multiple writes. The ADC SPI History will update show be updated to show the register writes executed in the script file.

3.3.2.1 ADS62PXX Frequently Used Registers

For ease of use, several buttons have been added that allow one-click register writes of commonly used features found in Table 3. These are found in the ADS62PXX tab, as these commands are specific to the ADS62PXX ADC only. The software writes to the ADC both the contents of the associated address and data when the button is clicked. When the ADS62PXX Reset button is pressed, it issues a software reset to the ADC, and it resets the button values to match the contents inside of the ADC. The graph indicator plots the SPI commands written to the ADC when a button has been depressed.

Table 3. ADS62PXX Frequently Used Registers

Default Value	Alternate Value
ADS62PXX Reset	
Over-ride bit: Off	Over-ride bit: On
2s Complement	Straight Binary
CMOS	DDR LVDS
Powerdown: OFF	Multiple Powerdown Options
No Course Gain	3.5-dB Course Gain
INT Reference	EXT Reference
Bit-Wise (LVDS Only)	Byte-Wise
Test Mode: None	Multiple Options
Fine Gain	Multiple Options

4 Connecting to FPGA Platforms

The ADS62PXX EVM provides several connection options to use the EVM with various FPGA development platforms and FPGA-based capture boards. The ADC features two output options, a DDR LVDS which easily interfaces with a TSW1200 capture card, and a CMOS output which interfaces with a TSW1100 capture card.

4.1 TSW1200

By default, the ADS62PXX EVM natively plugs into the TSW1200 FPGA platform. The TSW1200 Rev B and Rev C can be configured for capture support, allowing ADC analysis capability. For this option, please configure the ADS62PXX to output DDR LVDS data in an offset-binary fashion. User's should consult the TSW1200 documentation for configuration details. For users wishing to control the TSW1200 over the ADS62PXX SPI interface, move the surface-mount jumpers into the following positions. It should be noted that this is not needed for most evaluations, it is merely offered as a convenience option.

- Move the jumper on JP10 (SEN) to the 1–2 position, and remove R47 and populate R70 with a 0-Ω resistor.
- Move the jumper on JP8 (SCLK) to the 1–2 position, and remove R30 while installing the 0-Ω resistor to R69.
- Move the jumper on JP9 (SDATA) to the 1–2 position, and remove R33 while installing the 0-Ω resistor to R68.
- Move the jumper on JP11 to position 2–3 to configure the ADC into the SPI operation mode (serial interface mode).

4.2 TSW1100

When the ADS62PXX is configured in CMOS output mode users can use TI's TSW1100 capture board. Several additional board configuration steps are required before using this option.

- Remove resistor packs with the following reference designators: RN7, RN8, RN9, and RN10.
- Install TI's SN74AVC16244 buffer into U12 and U13.
- If using the parallel interface mode (JP11=1-2), configure the ADC in CMOS output mode using the silkscreen on JP14.

5 ADC Evaluation

This section describes how to set up a typical ADC evaluation system that is similar to what TI uses to perform testing for data-sheet generation. Consequently, the information in this section is generic in nature and is applicable to all high-speed, high-resolution ADC evaluations. This section covers signal tone analysis, which yields ADC data-sheet figures of merit such as signal-to-noise ratio (SNR) and spurious free dynamic range (SFDR).

5.1 Hardware Selection

To reveal the true performance of the ADC under evaluation, great care should be taken in selecting both the ADC signal source and ADC clocking source.

5.1.1 Analog Input Signal Generator

When choosing the quality of the ADC analog input source, consider both the harmonic distortion performance of the signal generator and the noise performance of the source.

In many cases, the harmonic distortion performance of the signal generator is inferior to that of the ADC, and additional filtering is needed if users expect to reproduce the ADC SFDR numbers found in the data sheet. Users can easily evaluate the harmonic distortion of the signal generator by hooking it directly to a spectrum analyzer, measuring the power of the output signal, and comparing that to the power of the integer multiples of the output signal frequency. If the harmonic distortion is worse than the ADC under evaluation, the ADC digitizes the performance of the signal generator and the true SFDR of the ADC is masked. To alleviate this, it is recommended that users provide additional LC filtering after the signal-generator output.

Another important metric when deciding on a signal generator is its noise performance. As with the distortion performance, if the noise performance is worse than that of the ADC under evaluation, the ADC digitizes the performance of the source. Noise can be broken into two components, broadband noise and close-in phase noise. Broadband noise can be improved by adding an LC filter to improve distortion performance; however, the close-in phase noise typically cannot be improved by additional filtering. Therefore, when selecting an analog signal source, it is important to review the manufacturer's phase noise plots and take care to choose a signal generator with the best phase-noise performance.

5.1.2 Clock Signal Generator

Equally important in the high-performance ADC evaluation setup is the selection of the clocking source. Most modern ADCs, the ADS62PXX included, accept either a sinusoidal or a square-wave clock input. The key metric in selecting a clocking source is selecting a source with the lowest jitter. This becomes increasingly important as the ADC input frequency (f_{in}) increases, because the ADC SNR evaluation setups can become jitter-limited (t_j) as shown by the following equation.

$$\text{SNR (dBc)} = 20 \log (2\pi \times f_{in} \times t_j(\text{rms}))$$

In theory, a square-wave source with femtosecond jitter would be ideal for an ADC evaluation setup. However, in practical terms, most commercially available square-wave generators offer jitter measured in picoseconds, which is too great for high-resolution ADC evaluation setups. Therefore, most evaluation setups rely on the ADC internal clock buffer to convert a sinusoidal input signal into a ultralow-jitter square wave. When selecting a sinusoidal clocking source, it has been shown that phase noise has a direct impact on jitter performance. Consequently, great scrutiny should be applied to the phase-noise performance of the clocking signal generator. TI has found that high-Q monolithic crystal filters can improve the phase noise of the signal generator, and these filters become essential elements of the evaluation setup when high ADC input frequencies are being evaluated.

5.2 Coherent Input Frequency Selection

Typical ADC analysis requires users to collect the resulting time-domain data and perform a Fourier transform to analyze the data in the frequency domain. A stipulation of the Fourier transform is that the signal must be continuous-time; however, this is impractical when looking at a finite set of ADC samples, usually collected from a logic analyzer. Consequently, users typically apply a window function to minimize the time-domain discontinuities that arise when analyzing a finite set of samples. For ADC analysis, window functions have their own frequency signatures or lobes that distort both SNR and SFDR measurements of the ADC.

TI uses the concept of coherent sampling to work around the use of a window function. The central premise of coherent sampling entails that the input signal into the ADC is carefully chosen such that when a continuous-time signal is reconstructed from a finite sample set, no time-domain discontinuities exist. To achieve this, the input frequency must be an integer multiple of the ratio of the ADC sample rate (f_s) and the number of samples collected from the logic analyzer (N_s). The ratio of f_s to N_s is typically referred to as the fundamental frequency (f_f). Determining the ADC input frequency is a two-step process. First, the users select the frequency of interest for evaluating the ADC; then, they divide this by the fundamental frequency. This typically yields a non-integer value, which should be rounded to the nearest odd, preferably prime, integer. Once that integer, or frequency bin (f_{bin}), has been determined, users multiply this with the fundamental frequency to obtain a coherent frequency to program into their ADC input signal generator. The procedure is summarized as follows.

$f_f = f_s/N_s$

$f_{bin} = \text{Odd\_round}(f_{desired}/f_f)$

Coherent frequency = $f_f \times f_{bin}$

6 Physical Description

This section describes the physical characteristics and PCB layout of the EVM.

6.1 PCB Layout

The EVM is constructed on a four-layer, 0.062-inch thick PCB using FR-4 material. The individual layers are shown in Figure 5 through Figure 8. The layout features a split ground plane; however, similar performance can be obtained with careful layout using a common ground plane.

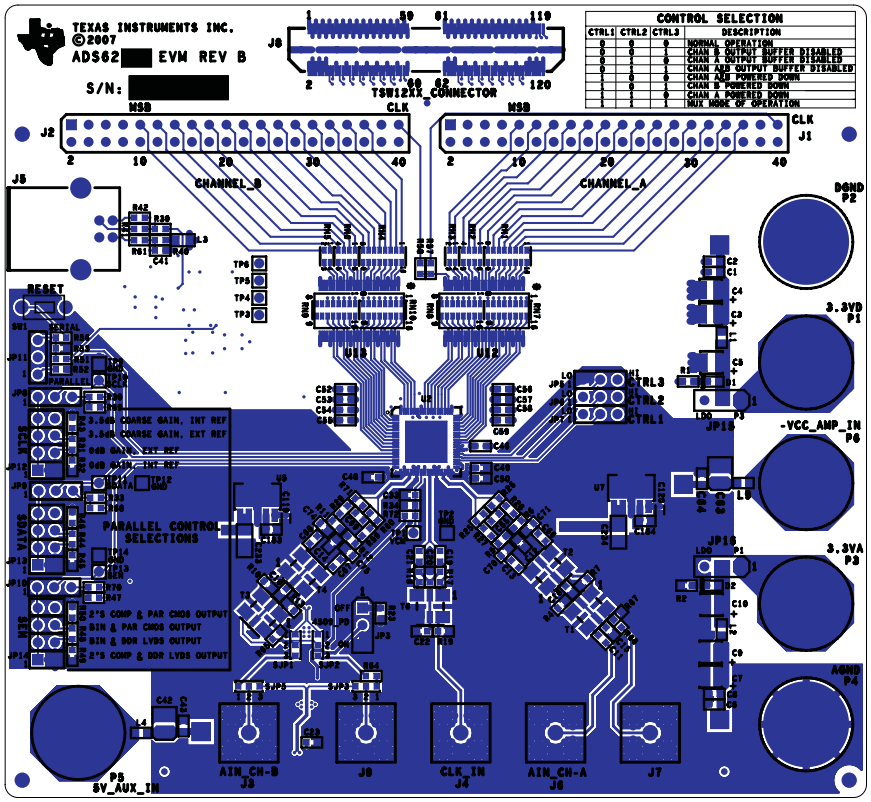

Figure 5. Top Silkscreen

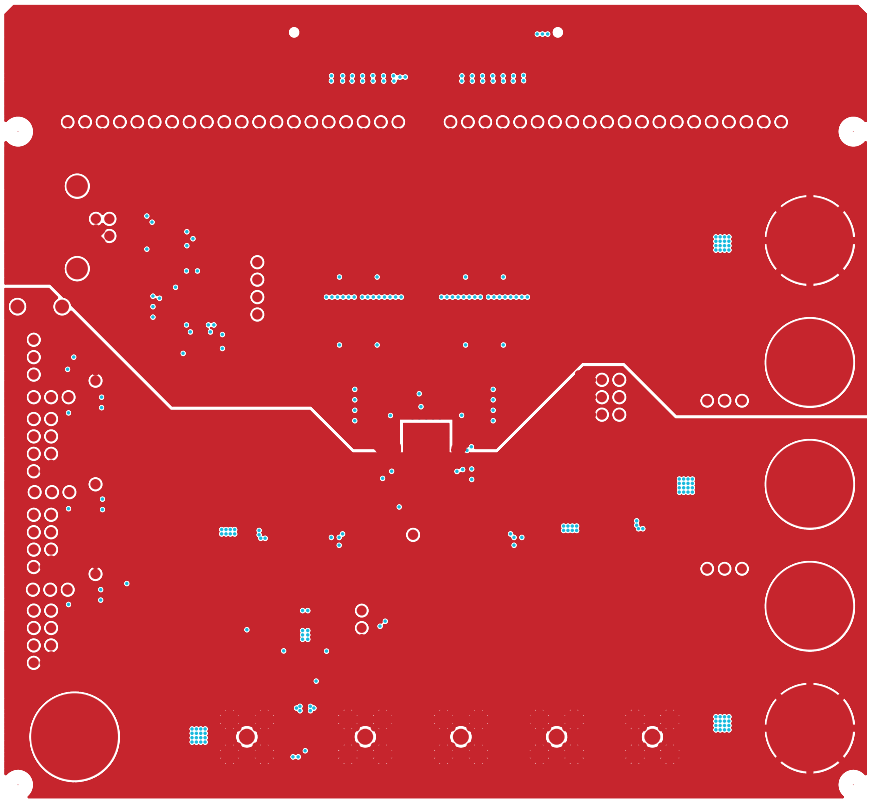

Figure 6. Component Side

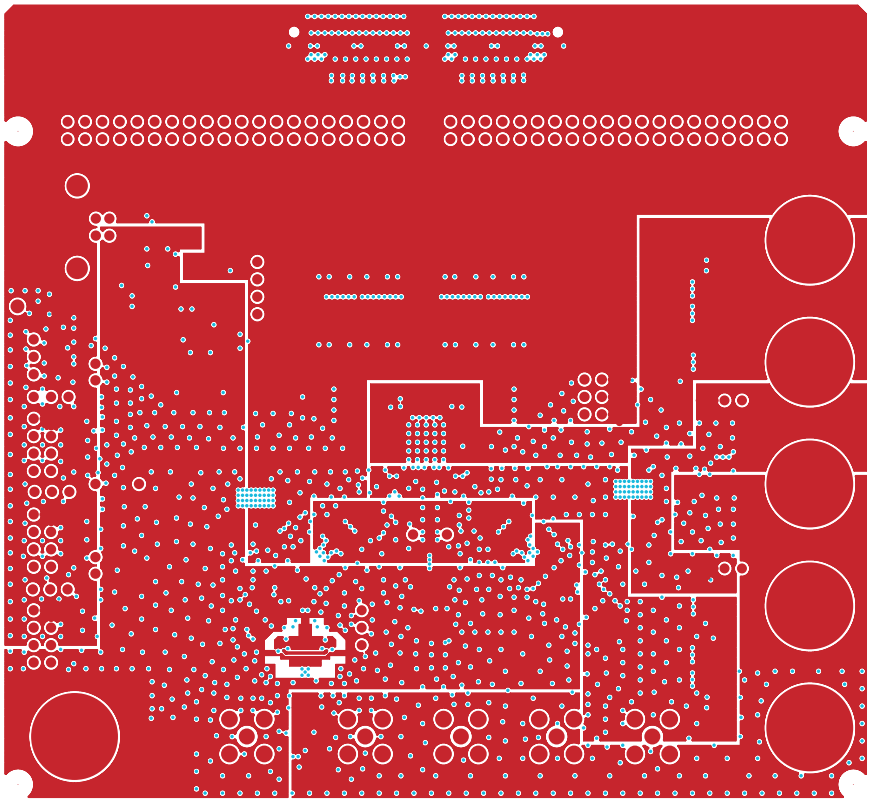

Figure 7. Power Plane 1

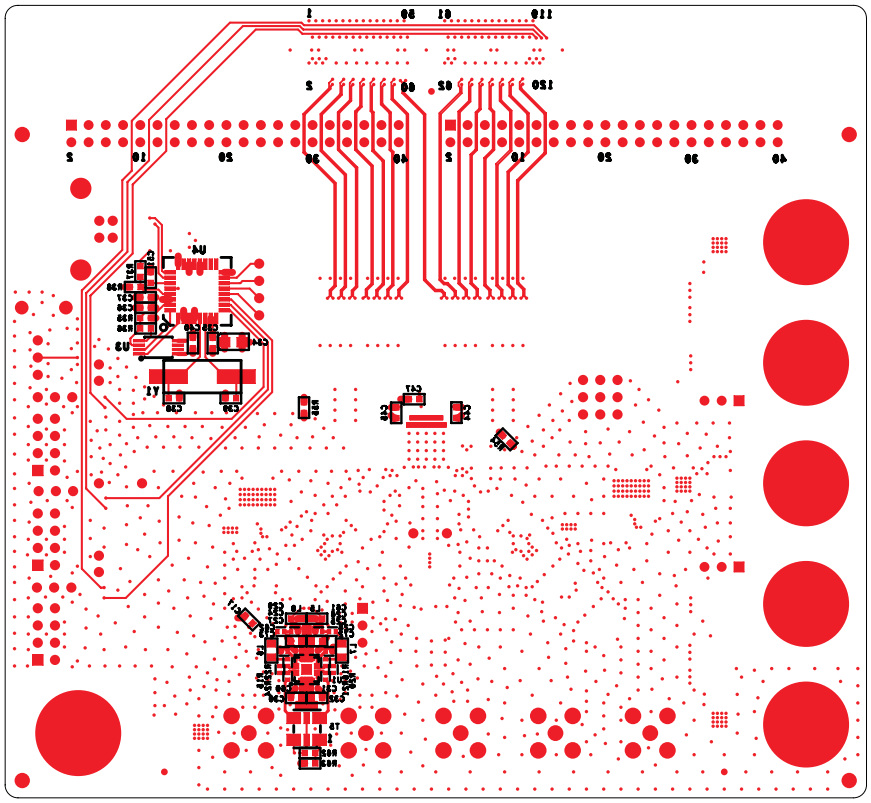

Figure 8. Bottom Side

6.2 Bill of Materials

Table 4. Bill of Materials

Qty	Reference	Value	Footprint	MFR	Part Number	DNI = Do Not Install
4	C1,C6,C43,C64	1µF	603	Panasonic	ECJ-1VB1A105K	
15	C2, C8, C19–C23, C52–C59	0.1µF	603	Panasonic	ECJ-1VB1C104K	
4	C3, C5, C7, C10	22µF	smd_cap_1210_pol	Kemet	T491A226M010AT	
2	C4, C9	10µF	smd_cap_1210_pol	Kemet	B45197A3106K209	
23	C11–C18, C33,C35–C37, C40,C44–C50, C66–C68	0.1µF	603	Murata	GRM188R71H104KA93D	
4	C24, C26, C30, C32	10µF	603	Murata	GRM188R60J106ME47D	
6	C25, C27, C31, C60, C72,C73	0.1µF	402	Panasonic	ECJ-0EB1C104K	
2	C28, C62	4.7pF	402	Panasonic	ECD-G0E4R7C	
2	C29, C61	5pF	402	Panasonic	ECJ-0EC1H050C	
1	C34	10µF	TANT_A	Kemet	T491A106M006AS	
2	C38, C39	27pF	603	Murata	GRM1885C2A270JA01D	
1	C41	0.01µF	603	Kemet	C0603C103K1RACTU	
2	C42, C63	33µF	TANT_B	Kemet	B45196H1336K209	
1	C51	33nF	603	AVX	06035C333KAT2A	
0	C65, C69	3.3pF	603	Panasonic	ECJ-1VC1H3R30C_DNI	DNI
4	C70, C71, C74, C75	5.6pF	603	AVX	06035A5R6CAT2A_DNI	DNI
2	C119, C120	0.01µF	402	Panasonic	ECJ-0EB1E103K	
2	C183, C184	1µF	603	Panasonic	ECJ-1V41E105M	
2	C233, C234	2.2µF	1206	Panasonic	ECJ-HVB1A225K	
2	D1, D2	GREEN	603	Panasonic	LNJ312G8TRA	
3	JP3, JP15, JP16	HEADER_1x3_100_430L		Samtec	HMTSW-103-07-G-S-.240	(SHUNT 2-3)
7	JP5–JP11	HEADER_1x3_100_430L		Samtec	HMTSW-103-07-G-S-.240	(SHUNT 1-2)
1	JP13	HEADER 4x2		Molex	90131-0124	
2	JP12, JP14	HEADER 4x2		Molex	90131-0124	(SHUNT 1-2)
2	J1, J2	HMTSW-120-07-G-D-.240		Samtec	HMTSW-120-07-G-D-.240	
4	J3, J4, J6, J9	SMA		Johnson Components	142-0701-201	
1	J5	CONN USB TYP B FEM		Milmax	897-43-004-90-000	
0	J7	SMA		Johnson Components	142-0701-201	DNI
1	J8	CONN_QTH_30X2-D-A		Samtec	QTH-060-02-F-D-A	
2	L1,L2	68 at 100MHz	603	Steward	MI0603J680R-10	
1	L3	1K at 100MHZ	805	Murata	BLM21AG102SN1D	
2	L4,L9	68 at 100MHz	603	Steward	MI0603J680R-10	
2	L5,L8	47nH	603	Coilcraft	0603CS-47NXJL	
2	L6,L7	150	805	API Delavan Inc	0805-151J	
1	P1	3.3VD		Allied Electronics	ST-351A	
1	P2	DGND		Allied Electronics	ST-351B	
1	P3	3.3VA		Allied Electronics	ST-351A	
1	P4	AGND		Allied Electronics	ST-351B	
1	P5	5V_AUX_IN		Allied Electronics	ST-351A	
1	P6			Allied Electronics	ST-351A	
2	RN1,RN4	22	rnet8_16_0603	CTS	742C163220JTR	
2	RN2,RN6	22	rnet4_8_0603	Panasonic	EXB-38V220JV	
2	RN3,RN5	22	rnet2_4_0603	Panasonic	EXB-34V220JV	
4	RN7–RN10	0 Ω	rnet8_16_0603	CTS	742C163000X	
2	R1,R2	750	603	Panasonic	ERJ-3EKF7500V	
8	R4–R7, R10–R13	49.9	603	Panasonic	ERJ-3EKF49R9V	
2	R15, R20	348	402	Panasonic	ERJ-2RKF3480X	
2	R16, R22	68	402	Yageo Corporation	RC0402FR-0768RL	
0	R17, R18	121	603	Panasonic	ERJ-3EKF1210V	DNI
1	R19	49.9	603	Panasonic	ERJ-3EKF49R9V	
2	R21, R24	100	402	Panasonic	ERJ-2RKF1000X	
1	R23	10K	603	Panasonic	ERJ-3EKF1002V	

Table 4. Bill of Materials (continued)

Qty	Reference	Value	Footprint	MFR	Part Number	DNI = Do Not Install
0	R25, R26, R60, R71	49.9	603	Panasonic	ERJ-3EKF49R9V_DNI	DNI
4	R27, R28, R29, R59	4.99	603	Yageo	RC0603FR-074R99L	
8	R30, R33, R34, R47, R54, R55, R61, R72	0 Ω	603	Panasonic	ERJ-3GEY0R00V	
9	R31, R32, R43–R46, R48–R50	1K	603	Panasonic	ERJ-3EKF1001V	
1	R35	10K	603	Panasonic	ERJ-3GEYJ103V	
1	R36	2.21K	603	Panasonic	ERJ-3EKF2211V	
1	R37	4.7K	603	Panasonic	ERJ-3GEYJ472V	
0	R38	10K	603	Panasonic	ERJ-3EKF1002V_DNI	DNI
1	R39	1.5K	603	Panasonic	ERJ-3EKF1501V	
0	R40, R68–R70	0 Ω	603	Panasonic	ERJ-3GEY0R00V_DNI	DNI
2	R41, R42	26.7	603	Panasonic	ERJ-3EKF26R7V	
2	R51, R56	10	603	Panasonic	ERJ-3EKF10R0V	
2	R52, R53	10K	603	Panasonic	ERJ-3EKF1002V	
2	R57, R58	22	603	Yageo	RC0603FR-0722RL	
0	R62, R64 ,R66	0 Ω	603	DALE	CRCW06030000Z0EA_DNI	DNI
3	R63, R65, R67	0 ohm	603	DALE	CRCW06030000Z0EA	
0	SJP1, SJP2	JUMPER_1x3_SMT	SMD_BRIDGE_1x3_0603	DNI	DNI	(SHUNT 2-3)
0	SJP3	JUMPER_1x3_SMT	SMD_BRIDGE_1x3_0603	DNI	DNI	(NO SHUNT)
0	SJP5	JUMPER_1x3_SMT	SMD_BRIDGE_1x3_0603	DNI	DNI	(SHUNT 1-2)
1	SW1	SW PUSHBUTTON	SW_RESET_PTS635	C & K Switch	PTS635SL43	
4	TP1, TP10, TP11, TP13	Test Point White	testpoint	Keystone	5002	
4	TP2, TP9, TP12,TP14	Test Point Black	testpoint	Keystone	5001	
4	TP3–TP6	T POINT R	TESTPOINT	Keystone	5002	
5	T1–T5	WBC1-1TL	XFMR_TC4-1W	Coilcraft	WBC1-1TL	
1	T6	TC1-1T	XFMR_TC4-1W	Minicircuits	TC1-1T	
1	U1	THS4509	QFN16	Texas Instruments	THS4509RGTT	
1	U2	ADS62PXX	QFN64	Texas Instruments	ADS62PXX	
1	U3	93C66B	TSSOP8	Microchip	93C66B	
1	U4	FT245BM	PQFP32	Future Technology Devices	FT245BM	
2	U5, U7	TPS79633DCQ	SOT_223_6_TG	Texas Instruments	TPS79633DCQ	
0	U12, U13	SN74AVC16244DGGR	TSSOP_48_496x244_20	Texas Instruments	SN74AVC16244DGGR_DNI	DNI
1	Y1	6.0000MHz	smd_csm-7_xtal	ECS	ECS-60-32-5PDN-TR	
10	Z_SH-H1	SHUNT-HEADER		Keltron	MJ-5.97-G or equivalent	SHUNT FOR HEADER
3	Z_SH-J1, Z_SH-J2, Z_SH-J5	SHUNT-JUMPER-0603		Panasonic	ERJ-3GE0R00X	SHUNT FOR JUMPER
4	Z_STANDOFF SCREW1,Z_STANDOFF SCREW2,Z_STANDOFF SCREW3,Z_STANDOFF SCREW4	PANHEAD SCREW 4-40 x 3/8		Building Fasteners	PMS 440 0038 PH	SCREW FOR STANDOFF
4	Z_STANDOFF1, Z_STANDOFF2,Z_STANDOFF3, Z_STANDOFF4	STANDOFF ALUM HEX 4-40 x .500		Keystone	2203	STANDOFF

6.3 EVM Schematics

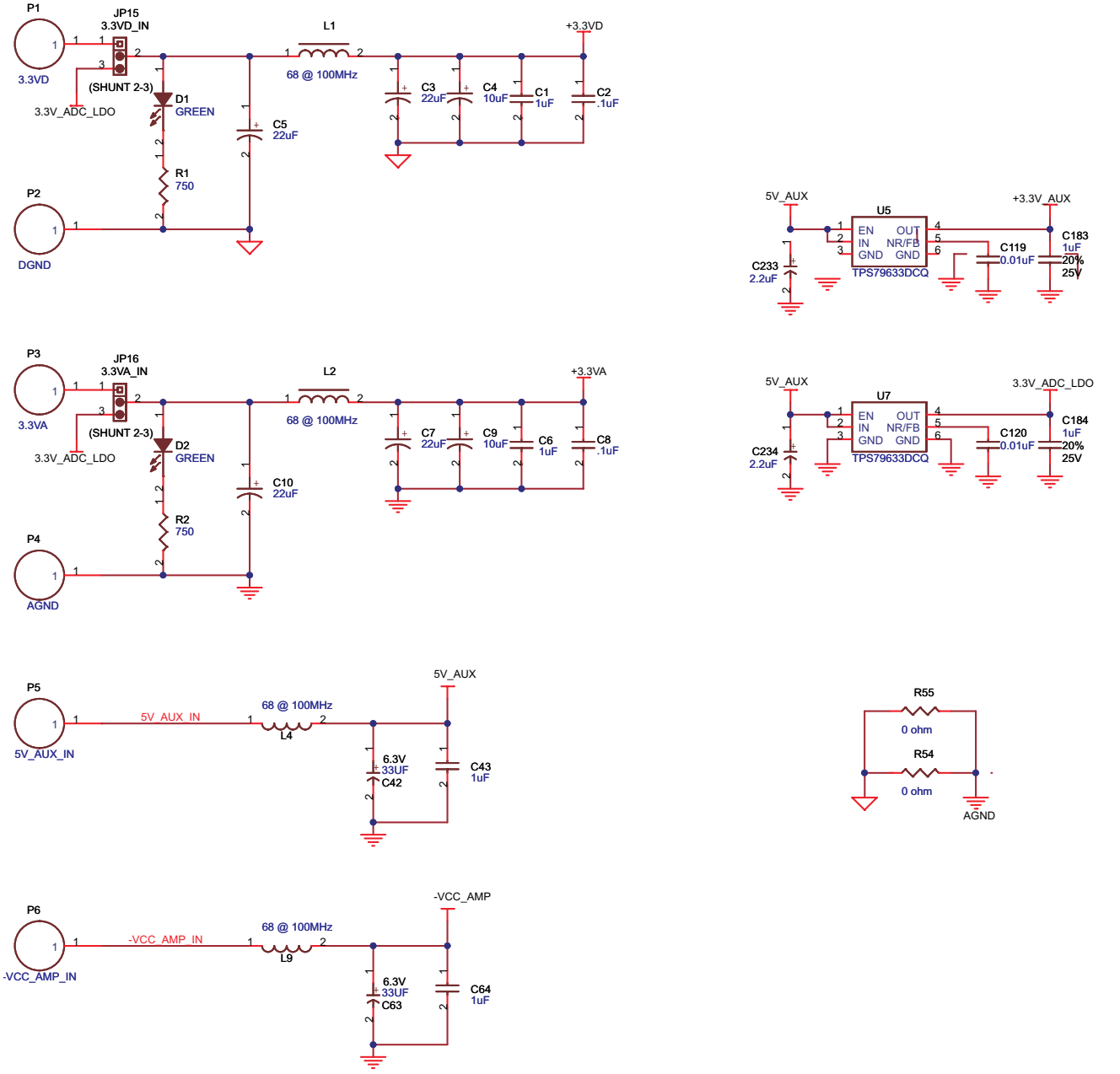

Figure 9. EVM Schematic, Sheet 1

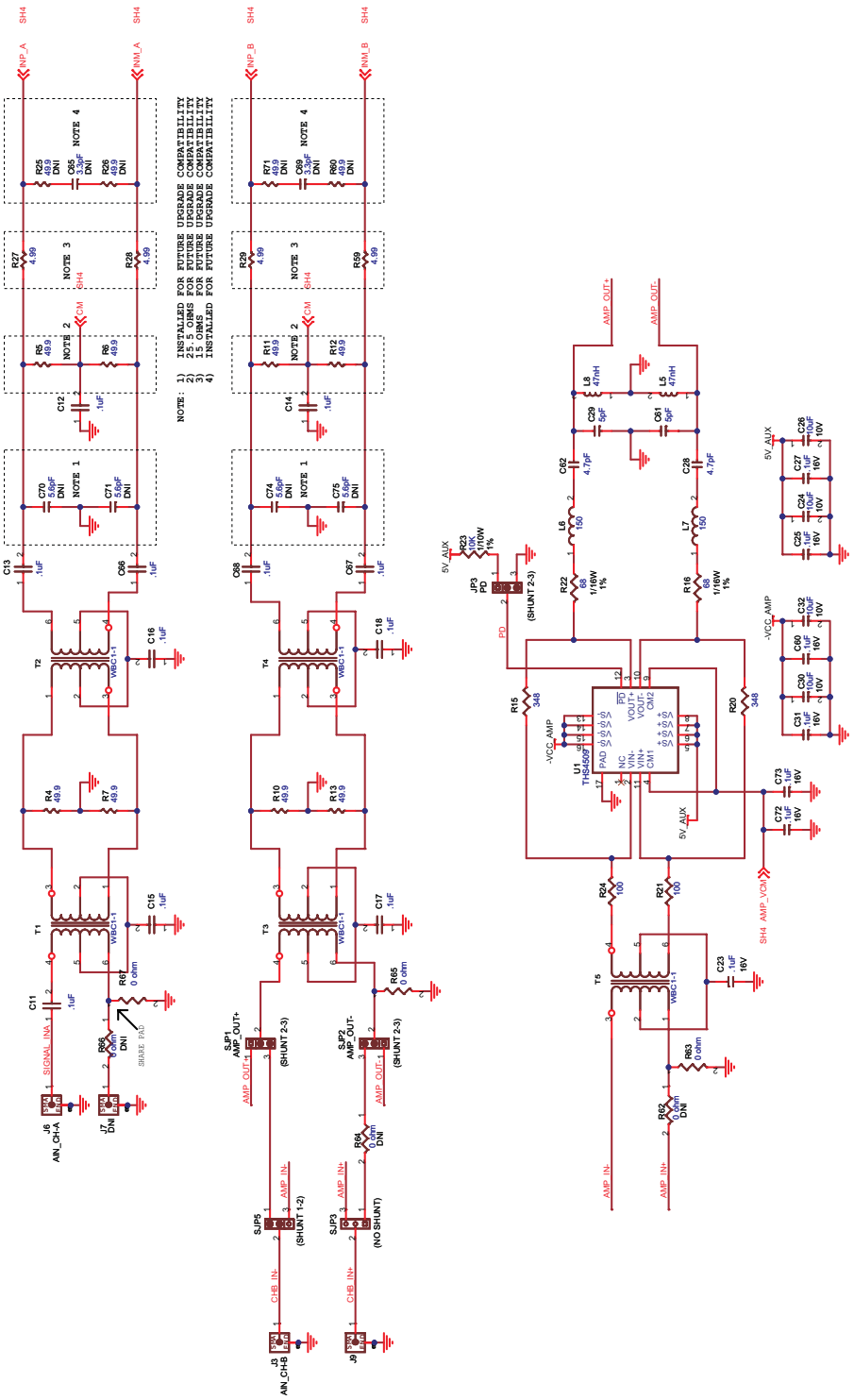

Figure 10. EVM Schematic, Sheet 2

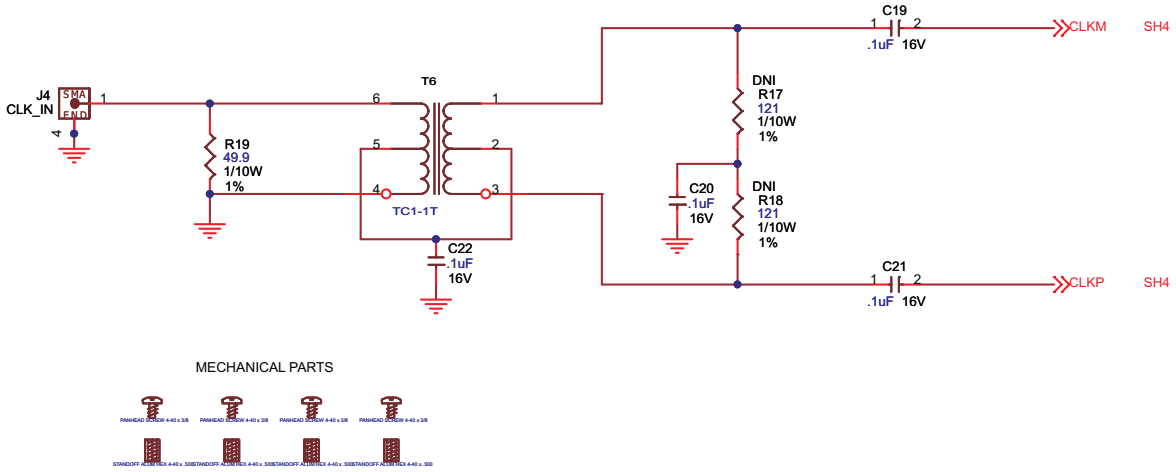

Figure 11. EVM Schematic, Sheet 3

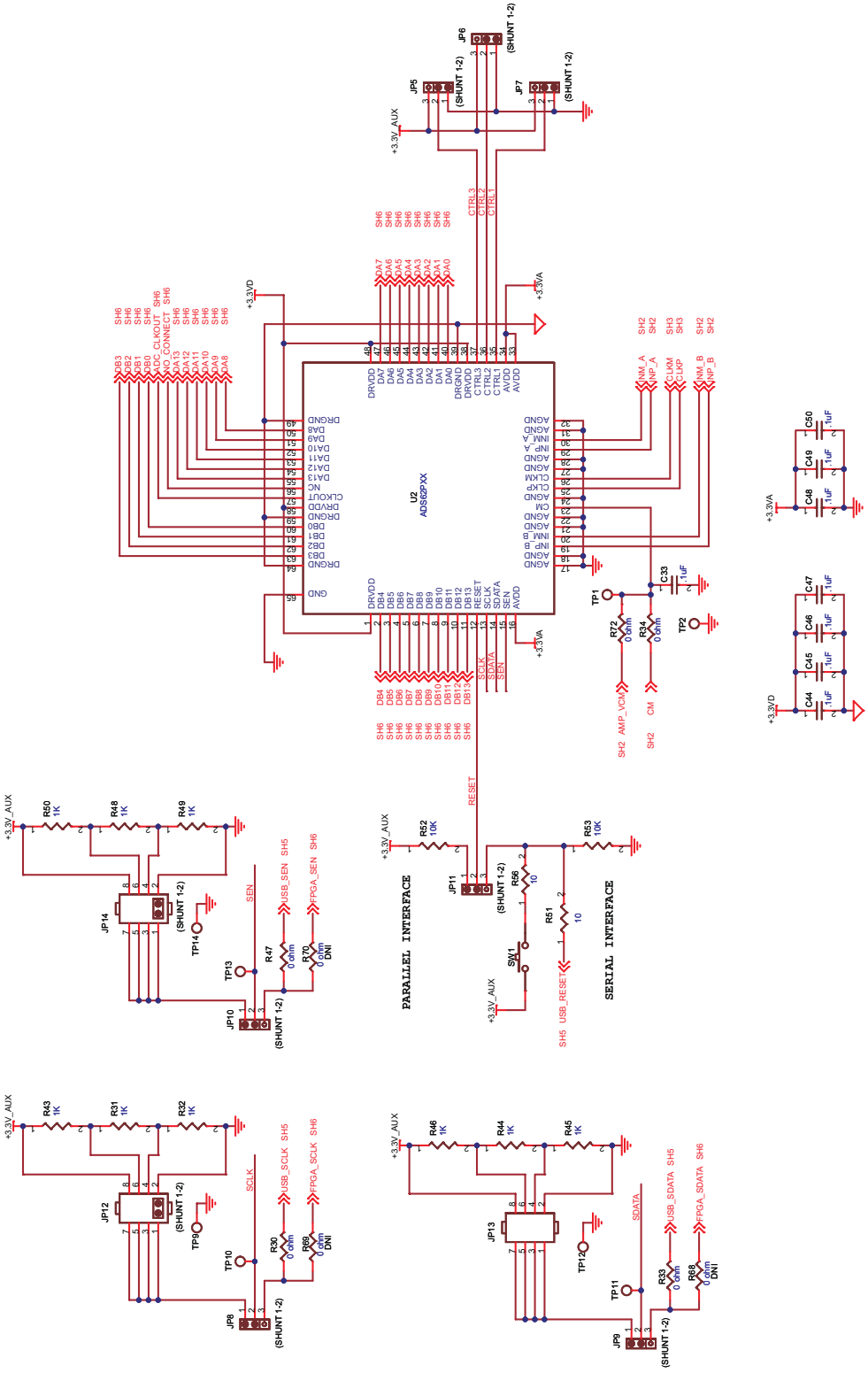

Figure 12. EVM Schematic, Sheet 4

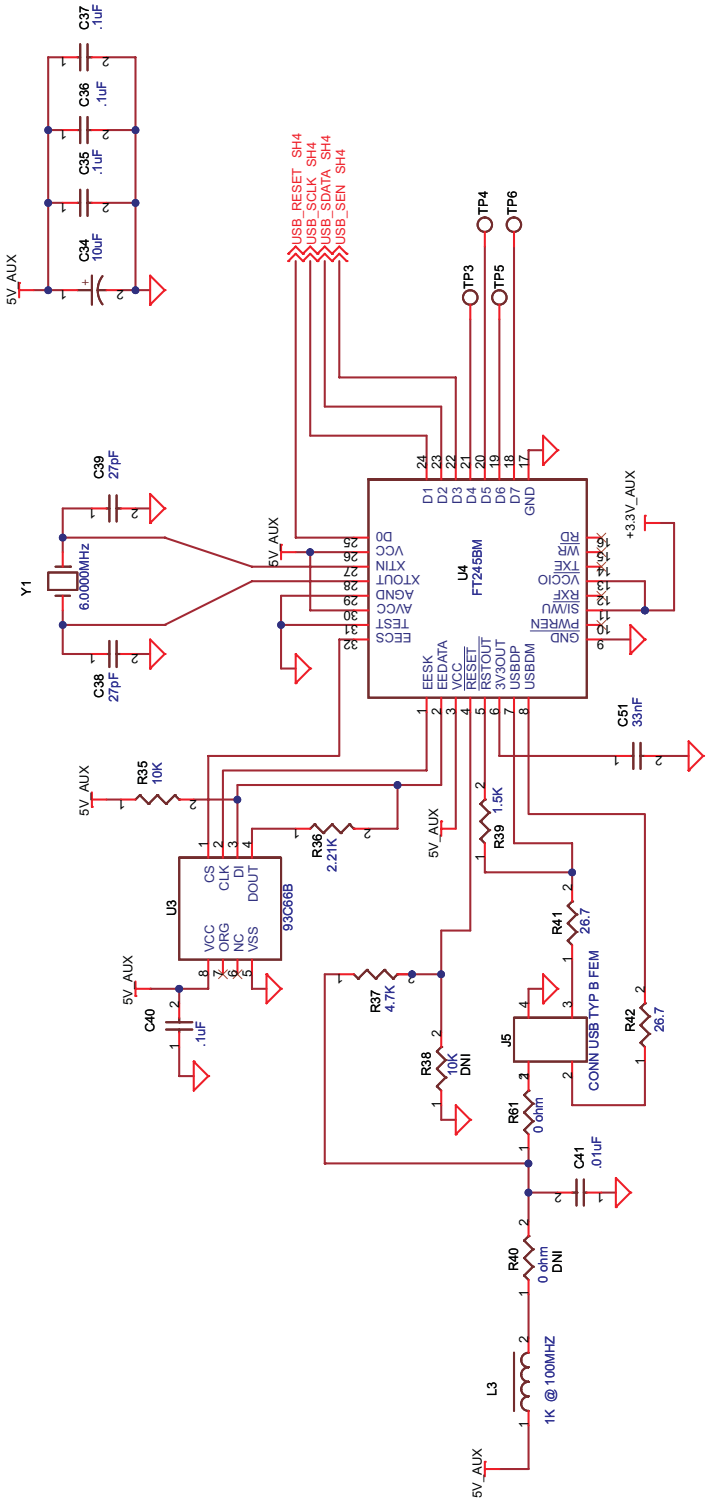

Figure 13. EVM Schematic, Sheet 5

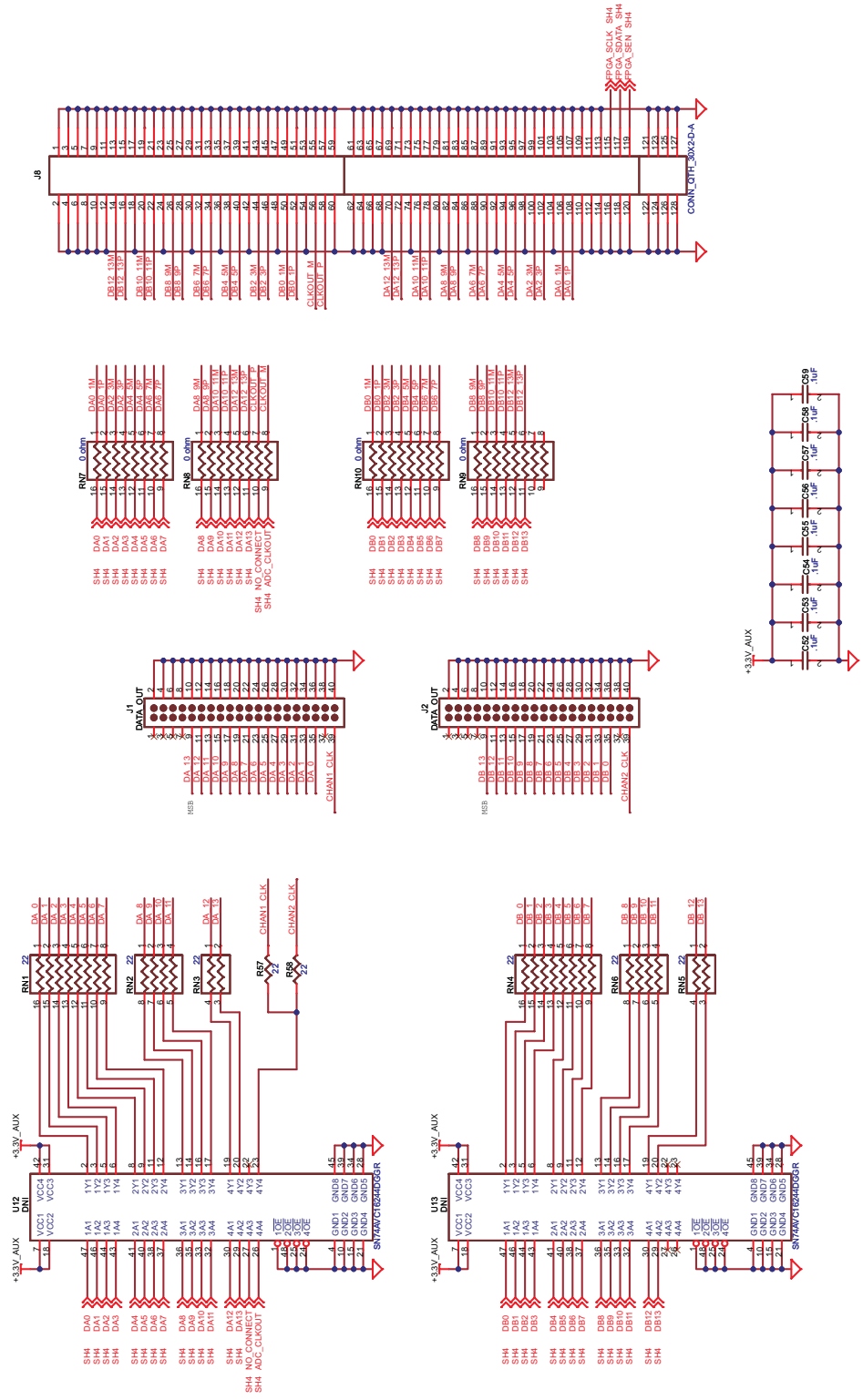

Figure 14. Breakout Board Schematic, Sheet 6

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Exceeding the specified input range may cause unexpected operation and/or irreversible damage to the EVM. If there are questions concerning the input range, please contact a TI field representative prior to connecting the input power.

Applying loads outside of the specified output range may result in unintended operation and/or possible permanent damage to the EVM. Please consult the EVM User's Guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative.

During normal operation, some circuit components may have case temperatures greater than 50°C. The EVM is designed to operate properly with certain components above 25°C as long as the input and output ranges are maintained. These components include but are not limited to linear regulators, switching transistors, pass transistors, and current sense resistors. These types of devices can be identified using the EVM schematic located in the EVM User's Guide. When placing measurement probes near these devices during operation, please be aware that these devices may be very warm to the touch.

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